REMARKS/ARGUMENTS

Claims 1-53 remain in the application, all of which stand rejected.

1. Rejection of Claims 1-13, 16, 17, 22-31, 34, 35, 39-47 and 50 Under 35 USC 103(a)

Claims 1-13, 16, 17, 22-31, 34, 35, 39-47 and 50 stand rejected under 35 USC 103(a) as being unpatentable over Jeong et al. (US 6,229,859 B1; hereinafter "Jeong") in view of Kirisawa (US 5,847,619).

With respect to claim 1, the Examiner asserts that Jeong teaches a graphical display of received data in col. 4, lines 3-11. Applicant agrees, but would like to clarify what it is that is actually displayed. Jeong states:

> . . .The frame aligner 110 receives the left-aligned data frames and the related flag information and outputs aligned data frames and output valid signal to the decoder 112. Finally, the decoder 112 receives the aligned data frames and output valid signal and decodes the aligned data frames to regenerate the original data and output the regenerated data as the received data (RX data). ***In a preferred embodiment, a liquid crystal display (LCD) controller chip receives the RX data from the decoder 112 and has the RX data displayed graphically on the display.***

Jeong, col. 4, lines 2-11 (emphasis added).

Although the above excerpt of Jeong teaches that received data (RX data) may be graphically displayed, it is noted that Jeong does not show what such a graphical display would look like. However, prior to Jeong's above indication that, in a "preferred embodiment", the RX data may be displayed, Jeong states:

> The encoder 102 receives original data to be transmitted (TX data) from a source (not shown). For example, ***the original data may be graphics data*** from a

> computer for display on a graphics monitor, and the encoder 102 may be embodied within a chip on a graphics card in the computer.
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> Jeong, col. 3, lines 12-16 (emphasis added).

Given the above two excerpts, which Jeong includes in a single discussion of FIG. 1 (see, col. 2, line 66 - col. 4, line 12), applicant believes it is fair to conclude that, in a "preferred embodiment", the displayed RX data mentioned in col. 4, line 11, is the graphics TX data mentioned in col. 3, line14. As such, it is unlcear how this graphics data would be displayed with "a representation of the set of data samples of. . .at least one analog signal in a correlated fashion", as recited in applicant's claim 1.

The nature of the RX data that is graphically displayed by Jeong is important because the Examiner admits that Jeong does not teach "displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion." This, the Examiner asserts, is taught by Kirisawa. More specifically, the Examiner indicates:

> . . .(See figs. 1 & 3 & col. 1, lines 30-34, col. 3, lines 25-45, col. 4, lines 57-63) Kirisawa discloses a system a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator.
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> Taking the combined teachings of Jeong and Kirisawa <u>as a whole</u>, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Jeong, in the manner as claimed and as taught by Kirisawa, for the benefit of analyzing the phase modulated signal.
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> 4/15/2008 Final Office Action, p. 4, sec. 3.

Applicant respectfully disagrees. The excerpts of Kirisawa cited by the Examiner state:

The vector network analyzer 109 measures the amplitude and phase of the RF modulated signal generated by modulation by the in-phase signal (I-signal) and in-quadrature phase signal (Q-signal) input to the quadrature phase modulator 100.

Col. 1, lines 30-34.

Referring to FIG. 3, a calibration system according to a first embodiment of the present invention is used for a quadrature phase modulator 10 which includes a local oscillator 11 for generating a carrier wave, a first mixer 12 for mixing I-signal with the carrier wave, a second mixer 13 for mixing Q-signal with a phase-corrected carrier wave obtained by shifting the carrier wave by 90º in phase, a 90º phase shifter 14 for phase-shifting carrier signal for the mixer 13, and a hybrid (H) block (or combiner) 15 for synthesizing the outputs of the mixers 12 and 13.

The calibration system comprises a sine-wave quadrature signal generator 20 for generating sine-wave quadrature signals having a phase difference of 90º therebetween, an adjusting block 30 integrated to the quadrature phase modulator 10 for adjusting the phase difference and amplitude difference between the sine-wave quadrature signals to supply the adjusted quadrature signals to the mixers 12 and 13 of the quadrature phase modulator 10, and a frequency spectrum analyzer for receiving the output of the quadrature phase modulator 10 to observe the frequency spectrum in the output of the quadrature phase modulator 10.

Col. 3, lines 25-45.

The spectrum analyzer 40 of the calibration system displays thereon the output of the quadrature phase modulator 10 in terms of frequency spectrum. While observing the frequency spectrum analyzer 40 or monitoring the output of the quadrature phase modulator, the quadrature phase modulator is calibrated. Calibration by the calibration system of the present embodiment will be described hereinafter.

Col. 4, lines 57-63.

Of note, none of the above excerpts say anything about displaying "***digital interface symbol information***" or displaying such digital interface symbol information "with a representation of the at least one analog signal ***in a correlated fashion***". Rather, the above excerpts only indicate that "the output of the quadrature phase modulator 10 in terms of frequency spectrum" can be displayed (col. 4, lines 57-63).

Kirisawa provides examples of the spectrum analyzer 40's display in FIGS. 7A-7D (col. 4, line 64 - col. 5, line 5). In these displays, it is noted that there is no display of "digital interface symbol information". In fact, there is no display of any digital information at all. Although Kirisawa does illustrate waveforms containing at least some digital information in FIGS. 5A and 5B (although not digital interface symbol information), it is noted that the waveforms shown in FIGS. 5A and 5B are representative of waveforms generated by the sin ROM 23 and cos ROM 24 of the quadrature signal generator 20 (see, FIGS. 3 & 4; and col. 3, lines 60-65). The waveforms shown in FIGS. 5A and 5B are not displayed on the spectrum analyzer 40, and the waveforms shown in FIGS. 5A and 5B are not correlated with any "digital interface symbol information".

For the reasons given above, applicant does not believe that Kirisawa teaches "displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion". However, assume for a moment that Kirisawa does teach "displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion". Even if this were so, applicant does not understand why one of ordinary skill in the art at the time of applicant's invention would have been combined Kirisawa's teachings with Jeong's. The Examiner asserts that it would have been obvious to incorporate Kiriswa's display technology into Jeong's system "for the benefit of analyzing the phase modulated signal". See, 7/10/2008 Final Office Action, p. 6. However, Jeong does not disclose a signal analysis system, but instead simply discloses a system for high-speed synchronized data communication (see Title). Furthermore, it is unclear how any sort of analysis display disclosed by Kirisawa would be integrated with the graphical display disclosed by Jeong (col. 4, lines 2-11) if the graphical display comprises "graphics data" generated by a graphics processor (col. 3, lines 12-16).

Because of the above-noted deficiencies of Jeong and Kirisawa, as well as the lack of motivation to combine their teachings, claim 1 is believed to be allowable over their combined teachings.

Claims 2-13, 16 and 17 are believed to be allowable, at least, because they depend from claim 1.

Claims 22-31, 34, 35, 39-47 and 50 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

2. Rejection of Claims 14, 15, 18-20, 32, 33, 36-38, 48, 49 and 51-53 Under 35 USC 103(a)

Claims 14, 15, 18-20, 32, 33, 36-38, 48, 49 and 51-53 stand rejected under 35 USC 103(a) as being unpatentable over Jeong in view of Kirisawa and Sajdak et al. (US 6,570,592 B1; hereinafter "Sajdak").

Applicant believes claims 14, 15, 18-10, 32, 33, 36-38, 48, 49 and 51-53 are allowable, at least, for reasons similar to why claim 1 is believed to be allowable, and because Sajdak fails to disclose that which is missing from Jeong and Voutilainen (see, e.g., Section 1 of these Remarks/Arguments).

3. Rejection of Claims 1, 22 and 39 Under 35 USC 103(a)

Claims 1, 22 and 39 stand rejected under 35 USC 103(a) as being unpatentable over Jeong in view of Iida (US 7,236,513 B2).

With respect to claim 1, the Examiner once again admits that Jeong fails to teach "displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion." However, the Examiner asserts that Iida teaches this in FIGS. 2A-N & col. 6, line 39 - col. 7, line 12. Applicant respectfully disagrees.

What is shown in Iida's FIGS. 2A-N are signals appearing at various different nodes of the transmitter 100 shown in FIG. 1. Iida contains absolutely no teaching that

any of the signals shown in FIGS. 2A-N are actually displayed in a correlated fashion. Iida certainly does not indicate that “digital interface symbol information [captured from a set of data samples for at least one analog signal is displayed] with a representation of the set of data samples of the at least one analog signal in a correlated fashion”, as is recited in applicant’s claim 1.

Because of the above-noted deficiencies of Jeong and Kirisawa, claim 1 is believed to be allowable over their combined teachings.

In response to the above arguments, the Examiner disagrees and indicates that:

> . . .Iida does teach displaying at least some of the digital interface symbol information (figs 2D & E “I & Q signals) with a representation of the at least one analog signal (figs. 2H & I “carrier signals”) in a correlated fashion. (figs 2J-M “I & Q signals modulating the carrier signal”)
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> 7/10/2008 Final Office Action, p. 4.

However, applicant believes the Examiner’s references to different figures showing different things is, in and of itself, illustrative of the fact that Iida does not teach ““displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion.”

Claims 22 and 39 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

4. Conclusion

In light of the amendments and remarks provided herein, applicant respectfully requests the issuance of a Notice of Allowance.

Respectfully submitted,
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